

What is claimed is:

1. A data slice circuit for separating data added  
to a prescribed signal of predetermined specifications  
superposed on a video signal based on a slice level,  
5 comprising:

a composite synchronous signal separation  
circuit for separating a composite synchronous signal  
from a video signal;

10 a line detection circuit for detecting a line  
on which a desired prescribed signal is superposed from  
the composite synchronous signal separation circuit and  
outputting a line detection pulse only during a period of  
the detected line;

15 a window pulse generation circuit for receiving  
the line detection pulse of the line detection circuit,  
outputting a pulse during a period for averaging the  
prescribed signal superposed on the detected line and  
changing a period for generating the pulse by the  
specifications of the superposed prescribed signal;

20 a data slice reference voltage detection  
circuit for sampling and holding an average voltage of  
the prescribed signal only during a period of the pulse  
output by the window pulse generation circuit and  
detecting a data slice reference voltage; and

25 a data slice level generation circuit for

generating the slice level by adding a direct current voltage to an output voltage of the data slice reference voltage detection circuit and changing the direct current voltage to be added in accordance with the line detected  
5 by the line detection circuit.

2. A data slice circuit as set forth in claim 1, wherein:

said prescribed signal is superposed on a video signal at a vertical blanking interval; and

10 said window pulse generation circuit generates a pulse becoming active during a period of a CRI signal when said prescribed signal includes a CRI signal and generates a pulse becoming active during a back porch immediately after a rise of a composite synchronous  
15 signal when a CRI signal is not included and only a reference signal is included.

3. A data slice circuit as set forth in claim 2, wherein said data slice reference voltage generation circuit outputs an average voltage value of a CRI signal  
20 when said prescribed signal includes a CRI signal and outputs a voltage value at a pedestal level when the CRI signal is not included and only a reference signal is included.

4. A data slice circuit as set forth in claim 2,  
25 wherein said data slice level generation circuit is

supplied with a first direct current voltage which is lower than the pedestal level and a second direct current voltage which is higher than the pedestal level, outputs an output voltage of said data slice reference voltage  
5 detection circuit as it is as a data slice level when said prescribed signal includes a CRI signal, and generates as a data slice level the output voltage at a level added with a voltage in accordance with a difference of said second direct current voltage and the  
10 first direct current voltage as a data slice level when the CRI signal is not included and only a reference signal is included.

5. A data slice circuit as set forth in claim 3, wherein said data slice level generation circuit is  
15 supplied with a first direct current voltage which is lower than the pedestal level and a second direct current voltage which is higher than the pedestal level, outputs an output voltage of said data slice reference voltage detection circuit as it is as a data slice level when  
20 said prescribed signal includes a CRI signal, and generates as a data slice level the output voltage at a level added with a voltage in accordance with a difference of said second direct current voltage and the first direct current voltage as a data slice level when  
25 the CRI signal is not included and only a reference

signal is included.

6. A data slice circuit for separating data added to a prescribed signal of predetermined specifications superposed on a video signal based on a slice level,

5 comprising:

a sync chip clamping circuit for performing sync chip clamping on a video signal;

10 a composite synchronous signal separation circuit for separating a composite synchronous signal from a video signal;

15 a line detection circuit for detecting a line on which a desired prescribed signal is superposed from the composite synchronous signal separation circuit and outputting a line detection pulse only during a period of the detected line;

20 a window pulse generation circuit for receiving the line detection pulse of the line detection circuit, outputting a pulse during a period for averaging the prescribed signal superposed on the detected line, and changing a period for generating the pulse by the specifications of the superposed prescribed signal;

25 a data slice reference voltage detection circuit for sampling and holding an average voltage of the prescribed signal clamped at the sync chip clamping circuit only during a period of the pulse output by the

window pulse generation circuit and detecting a data slice reference voltage; and

a data slice level generation circuit for generating the slice level by adding a direct current voltage to an output voltage of the data slice reference voltage detection circuit and changing the direct current voltage to be added in accordance with the line detected by the line detection circuit.

7. A data slice circuit as set forth in claim 6, wherein:

said prescribed signal is superposed on a video signal at a vertical blanking interval; and

said window pulse generation circuit generates a pulse becoming active during a period of a CRI signal when said prescribed signal includes a CRI signal and generates a pulse becoming active during a back porch immediately after a rise of a composite synchronous signal when a CRI signal is not included and only a reference signal is included.

8. A data slice circuit as set forth in claim 7, wherein said data slice reference voltage generation circuit outputs an average voltage value of a CRI signal when said prescribed signal includes a CRI signal and outputs a voltage value at a pedestal level when the CRI signal is not included and only a reference signal is

included.

9. A data slice circuit as set forth in claim 7,  
wherein said data slice level generation circuit is  
supplied with a first direct current voltage which is  
5 lower than the pedestal level and a second direct current  
voltage which is higher than the pedestal level, outputs  
an output voltage of said data slice reference voltage  
detection circuit as it is as a data slice level when  
said prescribed signal includes a CRI signal, and  
10 generates as a data slice level the output voltage at a  
level added with a voltage in accordance with a  
difference of said second direct current voltage and the  
first direct current voltage as a data slice level when  
the CRI signal is not included and only a reference  
15 signal is included.

10. A data slice circuit as set forth in claim 8,  
wherein said data slice level generation circuit is  
supplied with a first direct current voltage which is  
lower than the pedestal level and a second direct current  
20 voltage which is higher than the pedestal level, outputs  
an output voltage of said data slice reference voltage  
detection circuit as it is as a data slice level when  
said prescribed signal includes a CRI signal, and  
generates as a data slice level the output voltage at a  
25 level added with a voltage in accordance with a

difference of said second direct current voltage and the first direct current voltage as a data slice level when the CRI signal is not included and only a reference signal is included.